What is claimed is:

1. A trench capacitor process for preventing parasitic leakage, comprising the steps of:

providing a substrate with a trench formed therein, wherein the trench has a buried plate formed adjacent to the lower portion thereof;

forming a dielectric layer and a first conductive layer in the lower portion of the trench, wherein the buried plate and the first conductive layer are separated by the dielectric layer;

forming a doping layer on portions of each sidewall of the trench exposed by the dielectric layer and the first conductive layer to reveal portions of sidewalls of the trench in the upper portion;

forming a cap layer on each exposed sidewall and each doping layer;

performing an annealing process on each doping layer to forming a dopant region in the adjacent substrate, wherein each dopant region blocks leakage current resulted from a parasitic transistor adjacent to the trench and has a first distance from the surface of the substrate;

forming a second conductive layer in the trench to expose portions of the cap layers, wherein the second conductive layer contacts the first conductive layer and has substantially the same height with respect to the dopant regions;

removing portions of the cap layers exposed by the second conductive layer to reveal portions of the sidewalls in the upper portion of the trench; and

forming a third conductive layer on the second conductive layer to fill the trench, wherein the third conductive layer directly contacts the exposed sidewalls in the upper portions of the trench.

2. The trench capacitor process as claimed in claim 1, wherein the substrate is a p-substrate.

3. The trench capacitor process as claimed in claim 1, wherein the dielectric layer is nitride material.

4. The trench capacitor process as claimed in claim 3, wherein the nitride material is silicon nitride.

5. The trench capacitor process as claimed in claim 1, wherein the buried plate is an n-doped region in the substrate adjacent to the lower portion of the trench.

6. The trench capacitor process as claimed in claim 1, wherein the first conductive layer, the second conductive layer and the third conductive layer are n-doped polysilicon.

7. The trench capacitor process as claimed in claim 6, wherein the n-doped polysilicon is arsenic-doped polysilicon.

8. The trench capacitor process as claimed in claim 1, wherein the doping layer is boro-silicate-glass (BSG).

9. The trench capacitor process as claimed in claim 1, wherein the cap layer is silicon dioxide.

10. The trench capacitor process as claimed in claim 1, wherein the doping region is vertically distributed in the substrate adjacent to the trench and approximately equidistant from the trench.

11. The trench capacitor process as claimed in claim 1, wherein the annealing process is furnace annealing or rapid thermal annealing (RTA).

12. The trench capacitor process as claimed in claim 1, wherein the charging conductivity of the dopants in the doping region is the same as in the substrate.

13. The trench capacitor process as claimed in claim 1, wherein the concentration of the dopants in the doping region is about double that in the substrate.

14. The trench capacitor process as claimed in claim 1, wherein the first distance is about 500~2500Å.

15. A trench capacitor process for preventing parasitic leakage, capable of blocking leakage current resulting from a parasitic transistor adjacent to the trench, comprising the steps of:

forming a doping layer and a cap layer covering part of the sidewall of the trench; and

performing an annealing process on the doping layer and forming a dopant region in the substrate adjacent to the sidewall of the trench to block leakage current resulting from a parasitic transistor adjacent to the trench.

16. The trench capacitor process as claimed in claim 15, wherein the doping layer is boro-silicate-glass (BSG).

17. The trench capacitor process as claimed in claim 15, wherein the cap layer is silicon dioxide.

18. The trench capacitor process for preventing parasitic leakage as claimed in claim 15, wherein the charging conductivity of the dopants in the doping region is the same as that in the substrate.

19. The trench capacitor process as claimed in claim 15, wherein the concentration of the dopants in the doping region is about double that in the substrate.

20. The trench capacitor process as claimed in claim 15, wherein the dopant region does not contact the surface of the substrate and has a first distance therebetween.

21. The trench capacitor process as claimed in claim 20, wherein the first distance is about 500~2500Å.

22. A trench capacitor structure with an adjacent parasitic leakage channel comprising:

a node diffusion and a buried well in the substrate adjacent to a trench capacitor as a source or drain region;

a dual-layered dielectric layer on a sidewall of the trench capacitor as a gate dielectric and electrically contacting the node diffusion and the buried well;

a conductive layer on the dielectric layer to form a parasitic transistor adjacent to the trench capacitor;

a parasitic leakage channel of the parasitic transistor in the substrate between the node diffusion and the buried well; and

a dopant region in the substrate between the node diffusion and the buried well to elevate a threshold voltage for turning on the parasitic leakage channel.

23. The trench capacitor structure as claimed in claim 22, wherein the charging conductivity of the dopants in the doping region is the same as that in the substrate.

24. The trench capacitor structure as claimed in claim 22, wherein the concentration of the dopants in the doping region is about double that in the substrate.